Virtium
Solid State Storage and Memory

TuffDrive® CF – CompactFlash Card

PE Class, SLC, Industrial

VTDCFBPI004G-V11

Datasheet - Rev. 1.0

1. Description

Virtium's TuffDrive® CF is solid-state drive (SSD) technology in an industry-standard CompactFlash form factor designed for the unique capacity, workload and product lifecycle requirements of a broad range of embedded systems, including networking, industrial automation, medical equipment, gaming systems, point-of-sale terminals, data recorders and wearable computers.

Features

Capacity
- 4 GB

SLC NAND

Performance
- Sequential Read: 47 MB/s
- Sequential Write: 37 MB/s

Voltage Supply
- 5V ±10%
- 3.3V ±5%

Power Consumption(1)
- Typical: 0.75 W
- Maximum: 0.85 W
- Idle: 0.40 W

Temperature Ranges
- Industrial: -40ºC to 85ºC
- Non-Operating: -40ºC to 85ºC

Reliability
- MTBF: >4M hours
- Data retention: 10 years at new, 1 year at rated endurance
- 10,000 insertion cycle count

Supported
- Field upgradeable firmware functionality
- Optimized architecture for faster boot-up times.
- Built-in BCH ECC capable of correcting up to 96-bits in 1KB data.
- SMART Attribute Reporting

vtGuard® Power-Fail Protection
- Data protection during unexpected power-down
- Preserves static data through power loss event

Mechanical Dimensions
- Length x Width x Height mm (inches)
  36.40 (1.433) x 42.80 (1.685) x 3.30 (0.130)

Compliance
- CF 4.1 Standard compatible
- ATA-7 Standard compatible in TrueIDE Mode.
- PCMCIA 2.1
- RoHS

Environmental (Non-operating)
- Humidity (non-condensing): 5% to 95%
- Shock: 1500G, half-sine wave, 0.5ms duration
- Vibration: 20G, 20 Hz - 2000 Hz

(1) Based on a 5.0V power supply

Electrostatic Discharge (ESD) can damage this device. When handling the device, always wear a grounded wrist strap and use a static dissipative surface.

Any damage to the unit that occurs after its removal from the shipping package and ESD protective bag is the responsibility of the user.

Part Numbering System

V TD CFB P I 004G - V11

Where:	
V	= Virtium
TD	= TuffDrive
CFB	= Form Factor / Interface: CFB = CompactFlash Card
P	= Product Class: P = PE
I	= Operating Temperature: I = Industrial (-40ºC to 85ºC)
004G	= 4GB (1GB = 1,000,000,000 bytes)
V11	= Virtium Proprietary

2. Specifications

Capacity

Unformatted Capacity (GB)(1)	User-Addressable LBA(2)	User-Addressable Capacity Bytes
4	7,835,184	4,011,614,208
(1) 1GB = 1,000,000,000 bytes. LBA: Logical Block Address; Logical Block Size = 512 Bytes/1 Sector. (2) LBA: Logical Block Address; Logical Block Size = 512 Bytes/1 Sector.		

Performance(1)

Capacity (GB)	Sequential Read MB/s	Sequential Write MB/s
4	47	37
(1) CrystalDiskMark 7.0.0		

Power Requirements

Parameter	Min	Typ	Max
Voltage supply 5V (±10%)	4.50V	5.0V	5.50V
Voltage supply 3.3V (±5%)	3.14V	3.3V	3.47V

Parameter	Idle	Typical	Maximum
Power Consumption(1)	0.40 W	0.75 W	0.85 W
(1) Based on 100% Sequential Read / Write, 64K, 70/30 read/write workload @ 5.0V.			

Temperature and Humidity

Part Number	Operating Temperature	Non-Operating (1) Temperature	Moisture Sensitivity (Non-Condensing)
VTDCFBPI004G-V11	-40ºC to 85ºC	-40ºC to 85ºC	5% to 95%
(1) Maximum non-operating temperature assumes data is stored on the SSD. Temperatures above 85ºC are beyond NAND specification for data retention. Please see *Temperature Considerations for Industrial Embedded SSDs* whitepaper under the industrial SSD section of Virtium website (Virtium.com)			

Shock and Vibration

Reliability	Test Conditions	Reference Standards
Shock	1500G, half-sine wave, 0.5ms duration	JESD22-B110B.01
Vibration	20G, 20 Hz to 2000 Hz	JESD22-B103B.01

3. Reliability

Mean Time Between Failures (MTBF)

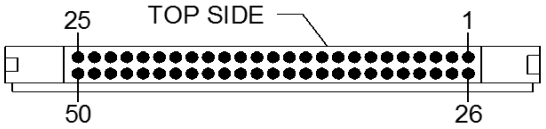
The SSD achieves a MTBF of greater than 4,000,000 hours predicted and is derived from the component reliability data using Telcordia SR-332 methods at 40ºC and tested under standard environmental operating conditions.

vtGuard® Power-Fail Protection

vtGuard® is an integrated power failure protection technology that will preserve data on the SSD if a sudden power failure should occur. It will also transfer the write cache (metadata, mapping tables) contents to the non-volatile flash and restore the contents upon power restoration. This data will be preserved regardless of the duration of the power failure event. This technology also ensures that the SSD will be recoverable after sudden power failure events although a rebuild of the mapping tables may delay readiness of the SSD on the ensuing power cycle on larger capacities.

4. Physical Specifications

Pin Layout / Assignments



Pin Layout

PC Card Memory Mode			PC Card I/O Mode			TrueIDE Mode		
Pin	**Name**	**I/O**	**Pin**	**Name**	**I/O**	**Pin**	**Name**	**I/O**
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O
28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O
31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CE2[1]	I
33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD	I	34	-IORD	I	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR[7] STOP[8,9]	I

PC Card Memory Mode			PC Card I/O Mode			TrueIDE Mode		
Pin	**Name**	**I/O**	**Pin**	**Name**	**I/O**	**Pin**	**Name**	**I/O**
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	READY	O	37	-IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL[5]	I	39	-CSEL[5]	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT[14] -DDMARDY[10] DSTROBE[11]	O	42	-WAIT[14] -DDMARDY[10] DSTROBE[11]	O	42	IORDY[7] -DDMARDY[8] DSTROBE[9]	O
43	-INPACK -DMARQ[12]	O	43	-INPACK -DMARQ[12]	O	43	DMARQ	O
44	-REG -DMACK[12]	I	44	-REG -DMACK[12]	I	44	-DMACK[6]	I
45	BVD2	O	45	-SPKR	O	45	-DASP	I/O
46	BVD1	O	46	-STSCHG	O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

Notes:

1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signal should be grounded by the host.
3. The signal should be tied to VCC by the host.
4. The mode is optional for CF+ Cards, but required for CF® Storage Cards.
5. The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6. If DMA operations are not used; the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition.
7. Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.
10. Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.
11. Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.
12. Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.
13. Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.
14. TuffDrive CF Series does not support the -WAIT signal.

Pin Descriptions

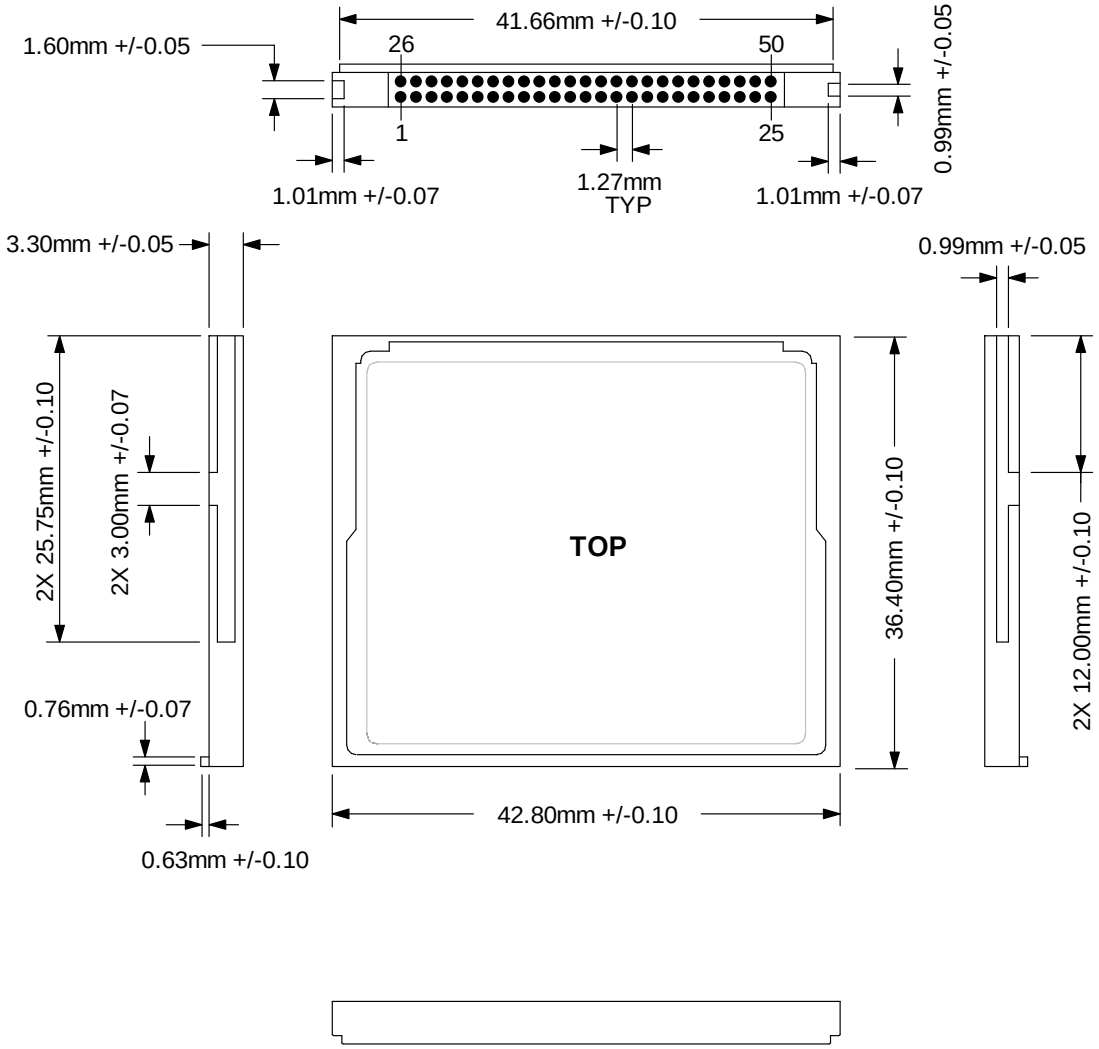
Pin No.	Pin Name	I/O	Mode	Description
8,10-12, 14-20	A10 – A0	I	PC Card Memory Mode	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CF® Storage Card or CF+ Card, the memory mapped port address registers within the CF® Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
8,10-12, 14-20	A10 – A0		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
18-20	A2 – A0		TrueIDE Mode	In True IDE Mode, only A [2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded to the host.
46	BVD1	I/O	PC Card Memory Mode	This signal is asserted high, as BVD1 is not supported.
	-STSCHG		PC Card I/O Mode	This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card configuration and Status Register.
	-PDIAG		TrueIDE Mode	In the TrueIDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
45	BVD2	I/O	PC Card Memory Mode	This signal is asserted high, as BVD2 is not supported.
	-SPKR		PC Card I/O Mode	This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
	-DASP		TrueIDE Mode	In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
26, 25	-CD1, -CD2	O	PC Card Memory Mode	These Card Detect pins are connected to ground on the CF Storage Card or CF+ Card. They are used by the host to determine that the CF Storage Card or CF+ Card is fully inserted into its socket.
			PC Card I/O Mode	This signal is the same for all modes.
			TrueIDE Mode	This signal is the same for all modes.
7, 32	-CE1, -CE2	I	PC Card Memory Mode	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, - CE2 allows 8 bit hosts to access all data on D0-D7.
	-CE1, -CE2		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-CS0, -CS1		TrueIDE Mode	In the TrueIDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits.
39	-CSEL	I	PC Card Memory Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			PC Card I/O Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			TrueIDE Mode	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the TrueIDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Pin No.	Pin Name	I/O	Mode	Description
31,30, 29,28,27 49,48,47, 23,22,21, 6,5,4,3,2	D15 - D00	I/O	PC Card Memory Mode	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
			PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
			TrueIDE Mode	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D [7:0] while all data transfers are 16 bit using D [15:0].
1, 50	GND		PC Card Memory Mode	Ground
			PC Card I/O Mode	Ground
			TrueIDE Mode	Ground
43	-INPACK	O	PC Card Memory Mode	This signal is not used in this mode.
	-INPACK		PC Card I/O Mode	The Input Acknowledge signal is asserted by the CF Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CF Storage Card or CF+ Card and the CPU.
	DMARK		TrueIDE Mode	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the host asserts -DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
34	-IORD	I	PC Card Memory Mode	This signal is not used in this mode.
	-IORD		PC Card I/O Mode	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CF Storage Card or CF+.
	-IORD		TrueIDE Mode	In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
	-HDMARDY			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate - HDMARDY to pause an Ultra DMA transfer.
	HSTROBE			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate - HDMARDY to pause an Ultra DMA transfer.

Pin No.	Pin Name	I/O	Mode	Description
35	-IOWR	I	PC Card Memory Mode	This signal is not used in this mode.
	-IOWR		PC Card I/O Mode	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CF Storage Card or CF+ Card controller registers when the CF Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
	-IOWR		TrueIDE Mode	In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
	STOP			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
9	-OE	I	PC Card Memory Mode	This is an Output Enable strobe generated by the host interface. It is used to read data from the CF Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
	-OE		PC Card I/O Mode	In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
	-ATA SEL		TrueIDE Mode	To enable True IDE Mode this input should be grounded by the host.
44	-REG	I	PC Card Memory Mode	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
			PC Card I/O Mode	The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
	-DMACK		TrueIDE Mode	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
41	RESET	I	PC Card Memory Mode	The CF® Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CF® Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
	RESET		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-RESET		TrueIDE Mode	In the TrueIDE Mode, this input pin is the active low hardware reset from the host.
13, 38	VCC		PC Card Memory Mode	+5 V, +3.3 V power.
			PC Card I/O Mode	+5 V, +3.3 V power.
			TrueIDE Mode	+5 V, +3.3 V power.
33, 40	-VS1, -VS2	O	PC Card Memory Mode	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CF® Storage Card or CF+ Card CIS can be read at 3.3V and -VS2 is reserved by PCMCIA for a secondary voltage.

Pin No.	Pin Name	I/O	Mode	Description
			PC Card I/O Mode	This signal is the same for all modes.
			TrueIDE Mode	This signal is the same for all modes.
42	-WAIT	O	PC Card Memory Mode	The -WAIT signal is driven low by the CF® Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
			PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	IORDY		TrueIDE Mode	In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
	-DDMARDY			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.
	DSTROBE			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-outburst.
36	-WE	I	PC Card Memory Mode	This is a signal driven by the host and used for strobe memory write data to the registers of the CF® Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
			PC Card I/O Mode	In PC Card I/O Mode, this signal is used for writing the configuration registers.
			TrueIDE Mode	In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
24	WP	O	PC Card Memory Mode	Memory Mode: The CF® Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
	-IOIS16		PC Card I/O Mode	I/O Operation: When the CF® Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
	-IOCS16		TrueIDE Mode	In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Mechanical Dimensions



Note:
1. All dimensions are in millimeters
2. The dimensional diagram is for reference only

5. Software Interface

TuffDrive CF VTDCFB Series products are fully compliant with the CFA Specification, Revision 4.1.

Please reference the CFA Specification, Revision 4.1 for Software Interface details or contact Virtium for the full specification.

SMART Command Support

The controller firmware supports the following SMART commands, determined by Feature Register value

Value	Command
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status

SMART Data Structure

The following 512 bytes comprise the SMART data structure of the device. Users can obtain the data using the Read Data (D0h) command.

Offset	Value	Description
0 - 1	XXXh	SMART structure version.
2 - 361		Attribute entries 1 to 30 (12 bytes each).
362	00h	Off-line data collection status (no off-line data collection).
363	00h	Self-test execution status byte (self-test completed).
364 - 365	0000h	Total time to complete off-line data collection.
366	00h	Vendor Specific
367	XXh	Off-line data collection capability (no off-line data collection).
368 - 369	XXh	SMART capabilities.
370	XXh	Error logging supported bit 0 = 1.
371	XXh	Vendor Specific
372		Short self-test routine recommended polling time.
373		Extended self-test routine recommended polling time.
374		Conveyance self-test routine recommended polling time.
375 - 385		Reserved
386 - 395		FW Version Number
396 - 399		Reserved
400 - 406	Fixed	TBD
407 - 511		Reserved

SMART Attributes

The following table defines the current SMART data attributes that are supported.

Attribute ID (Hex)	Attribute ID (Dec)	Attribute Name	Description
0C	12	Power Cycle Count	Number of Power On Cycles
C2	194	Temperature	Not used.
C4	196	Spare Block Count	The amount of available spare blocks. The attribute value returned is the percentage of remaining spare blocks summed over all flash chips, i.e.,(100 × Current Spare Blocks / Initial Spare Blocks).
C7	199	UDMA CRC Error Rate	Not used but included for compatibility.
CB	203	ECC Error Count	Total number of ECC errors correctable and uncorrectable for the NAND data.
0CC	204	Number of Corrected ECC Errors	The total number of correctable ECC errors that have occurred on flash read commands.
D5	213	Reserved	Reserved
D6	214	Reserved	Reserved
E5	229	Erase Count	The value returned is an estimation of the remaining card life, expressed as a percentage according to the number of flash block erases compared to the target number of erase cycles per block.
E8	232	Number of Reads	The total number of flash read commands.
F1	241	Total LBAs Written	Total number of LBAs written to the disk, divided by 65536.
F2	242	Total LBAs Read	Total number of LBAs read from the disk, divided by 65536.

6. Certifications and Compliance

Compliance / Certification	Description
CE and FCC Compliant	Class: FCC Part 15 Subpart B Class B:2011 Declaration of Conformity registration No. STE120607699
RoHS Compliant	Restriction of Hazardous Substance Directive
UL Certified	Underwriters Laboratories, Inc. 94V-0
WEEE Certified	Waste, Electrical and Electronic Equipment Directive
ISO-9001 AS9001 Rev. C Certificate	Quality Management
ISO-14001 Certificate	Environmental Management

7. Contact Information

Corporate Headquarters and Manufacturing Location:
30052 Tomas, Rancho Santa Margarita, CA 92688 USA

Main Website:	www.virtium.com
Contacts / Sales:	http://www.virtium.com/contacts-sales/
Toll Free:	(888) VIRTIUM / (888) 847.8486
Telephone:	1+ (949) 888.2444
Fax:	+1 (949) 888.2445
Customer Support	custserv@virtium.com

8. Revision History

Date	Revision	Page(s)	Description
03/11/2021	1.0	All	Initial release

Virtium manufactures storage and memory and solutions for the world's foremost industrial embedded OEMs. For over two decades, we have designed, manufactured and supported our products in the USA – fortified by a network of global locations. Our world-class technology and unsurpassed support provide a superior customer experience that continuously results in better industrial embedded products for an increasingly interconnected world.